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**IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
ON APPEAL FROM THE EXAMINER TO THE BOARD
OF PATENT APPEALS AND INTERFERENCES**

In re Application of:	Shriniwas Lohia
Serial No.:	09/436,920
Filing Date:	November 9, 1999
Examiner:	Adnan M. Mirza
Group Art Unit:	2141
Title:	SYSTEM FOR COMMUNICATING MANAGEMENT INFORMATION AND METHOD OF OPERATION

Board of Appeals and Interferences
United States Patent and Trademark Office
PO Box 1450
Alexandria, VA 22313-1450

Dear Sir:

REQUEST FOR REHEARING PURSUANT TO 37 C.F.R. § 41.52(a)(1)

Applicant respectfully requests a rehearing before the Board of Patent Appeals and Interferences ("the Board") regarding the above-identified patent application, on which the Board issued a written opinion dated May 24, 2005 ("Decision").

According to 37 C.F.R. § 41.52(a)(1), an "[a]ppellant may file a single request for rehearing within two months of the date of the original decision of the Board." Furthermore, § 41.52(a)(1) specifies that "[t]he request for rehearing must state with particularity the points believed to have been misapprehended or overlooked by the Board."

Consequently, Applicant respectfully submits, in accordance with 37 C.F.R. § 41.52(a)(1), that the Board has misinterpreted the teachings of the *Flood* reference. At the outset, in an effort to help articulate the Applicant's more specific arguments below, Applicant would like to draw the Board's attention to the description of system controller 16 in Figure 3 and the corresponding text of *Flood*, as Applicant believes that certain details of

the operation of system controller 16 have inadvertently escaped the Board's notice. As *Flood* explains, and as is documented with citations below, terminal 24 connects to system controller 16 through either line driver 52 or line driver 54 and communicates information to random access memory (RAM) 38 of system controller 16 over communication buses 31-33. System controller 16 may subsequently use and disseminate this information to administer program changes in the corresponding program execution modules 18, including to download user programs. Significantly, however, communication arbitration circuit 40 of system controller 16 ensures that only a single device is communicating on communication buses 31-33 at a particular time. Thus, to whatever extent programming modules 18 may also communicate on communication buses 31-33 (e.g. by coupling indirectly to communication buses 31-33 through backplane buses 21-23 and/or other components of system controller 16), they are not able to do so concurrently with terminal 24. As a result, no "communication link" is ever formed between terminal 24 and any of program execution processors 18 or I/O scanners 20.

In light of these details of the operation of *Flood* and their significance, as discussed more thoroughly below, Applicant respectfully notes that the Board has overlooked and/or misapprehended the following facts:

No "communication link" is established between terminal 24 and processing modules 18.

In sustaining the Examiner's rejection, the Board states that:

> Although cable 25 is not connected in response to a command, the appropriate connection along the control data and address lines between the system controller 15 and the designated programmable controller is made in response to the commands received on cable 25 from the client. We find that this operation meets the recitations of claim 1. In other words, individual communication links are established between system controller 16 and execution processors 18 on lines 21-23 in response to requests made by the client at terminal 24. *Decision*, p. 7.

To the extent that the Board is equating the terminal 24 of *Flood* with the "client" of Claim 1, the "individual communication links" described by the Board are not formed between terminal 24 and execution processors 18. Although the Board does not provide any citation to identify the portion of *Flood* the Board is relying upon, Figure 3 of *Flood* and the

corresponding text clearly indicate that, to whatever extent any form of communication link is established *between system controller 16* and execution processors 18, the programmable controller 10 of *Flood* never "establish[es] a communication link" *between terminal 24* and execution processors 18 as required by Claim 1.

More specifically, terminal 24 connects to system controller 16 through one of line drivers 52 and 54 and, in particular, couples to communication buses 21-23 through line driver 52 and 54 and serial input/output controller (SIO) 48. Column 7, lines 11-16. Also located on communication buses 31-33 is RAM 38, which is "for temporary storage of data received from or to be sent to the various external devices connected to the system controller." Moreover, "[a direct memory access (DMA)] circuit 42 allows the SIO 48 to access RAM 38 to store or obtain data which have been received or will be transmitted over their respective external communication channels." Column 7, lines 31-35. Thus, data communicated to system controller 10 by terminal 24 is transmitted to RAM 38 over communication buses 31-33.

Significantly, however, to whatever extent execution processors 18 may have direct access to RAM 38, they are not able to access communication buses 31-33 while terminal 24 is communicating on communication buses 31-33. As *Flood* indicates:

> Access to the communication buses 31-33 is controlled by an arbitration circuit 40 which resolves conflicts when several devices request access to these busses at the same time. The arbitration circuit 40 determines which component of the communication section will have access to the shared buses 31-33. A device seeking the buses sends a request signal to the arbitration circuit 40 via a line of the control bus 31 and the arbitration circuit grants the request to one device at a time by producing an access signal on another control line for that device.
>
> Column 7, lines 36-46.

Thus, to whatever extent execution processors 18 directly access RAM 38 over communication buses 31-33, execution processors 18 do not communicate over communication buses 31-33 concurrently with terminal 24 and only one device may be transmitting data to or receiving data from RAM 38 at a time. As a result, no "communication link" is established between client 24 and execution processors 18.

Any alleged communication links established between system controller 16 and execution processors 18 are not "established . . . *between [a] client* and a particular one of [a] first interface card and a second interface card"

Applicant also respectfully submits that, to whatever extent the Board may be instead equating alleged communication links *between system controller 16* and execution processors 18 with the "communication links" claimed by Claim 1, any alleged communication links established between system controller 16 and execution processors 18 cannot be viewed as being established "between [a] client and a particular one of [a] first interface card and [a] second interface card" as recited by Claim 1. Applicant respectfully notes that the Board claims to maintain the Examiner's mapping of elements with respect to the "client" and "management card" of Claim 1, equating terminal 24 of *Flood* with the "client" and system controller 16 with the "management card." *Decision*, p. 6. Thus, even accepting, for the sake of argument, the accuracy of this mapping, any alleged "communication links" established between the system controller 16 and any execution processor 18 would represent communication links between the "management card" and the "first interface card" or the "second interface card," rather than communication links between the "client" and the "first interface card" or the "second interface card," as required by Claim 1. As a result, although Applicant respectfully notes that the Board has failed to cite to any portion of *Flood* that describes such communication links, any such communication links would not represent communication links "established . . . *between the client* and the first interface card and the second interface card" (emphasis added) as required by Claim 1.

Thus, Applicant has identified one or more factual errors that serve as a basis for the Decision. In light of the fact that, to maintain a rejection for lack of novelty under 35 U.S.C. § 102, "[t]he identical invention must be shown in as complete detail as is contained in the ... claim," *Richardson v. Suzuki Motor Co.*, 868 F.2d 1226, 1236, 9 U.S.P.Q.2d 1913, 1920 (Fed. Cir. 1989) (emphasis added), and "[t]hese elements must be arranged as in the claim under review," *In re Bond*, 910 F.2d 831, 831, 15 U.S.P.Q.2d 1566, 1567, (Fed. Cir. 1990) (emphasis added), these factual mistakes are clearly significant to the ultimate ruling of the Board. Additionally, Applicant is filing this request on or before July 24, 2005, which is

within two months of the Board's Decision. Applicant has made no such previous request in this patent application. As a result, Applicant respectfully notes that Applicant has satisfied the criteria for filing this request for rehearing in accordance with § 37 C.F.R. § 41.52(a)(1).

CONCLUSION

In accordance with 37 C.F.R. § 41.52(a)(1), Applicant respectfully submits that the Board misinterprets or overlooks either or both of the following facts:

1). No "communication link" is established between terminal 24 and processing modules 18.

2). Any alleged communication links established between system controller 16 and execution processors 18 are not "established . . . *between [a] client* and a particular one of [a] first interface card and a second interface card"

As a result, Applicant respectfully requests rehearing of the present appeal under 35 U.S.C. 6(b). Although no fees are believed to be required by this request, the Commissioner is hereby authorized to charge any fees or credit any overpayments to Deposit Account No. 02-0384 of Baker Botts L.L.P.

Respectfully submitted,

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Date: July 22, 2005

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PATENT APPLICATION

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

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Dear Sir:

CERTIFICATE OF MAILING BY EXPRESS MAIL

I hereby certify that the attached Request for Rehearing, Baker Botts return postcard, and this Certificate of Mailing are being deposited with the United States Postal Service "Express Mail Post Office to Addressee" service under 37 C.F.R. § 1.10 on this 22nd day of July 2005 and is addressed to the Board of Appeals and Interferences, United States Patent and Trademark Office, PO Box 1450, Alexandria, VA 22313-1450.

Willie Jiles
Willie Jiles

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